C'

at least one electro-mechanically polished metal layer formed over said substrate, said electro-mechanically polished metal layer having a reduced number of cavities and/or scratches.

---

43. (Twice Amended) A semiconductor capacitor comprising:

C2

Sub D2

a bottom electrode formed over a substrate;

an insulating layer formed over said bottom electrode; and

a top electrode formed over said insulating layer, wherein at least one electrode surface comprises an electro-mechanically polished surface, said electro-mechanically polished surface having a reduced number of cavities and/or scratches.

Sub D3

C3

48. (Amended) A processor system comprising:

a processor; and

a memory device electrically coupled to said processor, said memory device comprising a substrate; and

a capacitor formed over said substrate, said capacitor comprising at least one electro-mechanically polished layer provided over said substrate, wherein said electro-mechanically polished layer has a reduced number of cavities and/or scratches.

Please add new claims 49-51.

Sub D4

49. (New) A semiconductor device comprising:

a substrate; and

at least one electro-mechanically polished noble metal layer formed over said substrate.

C4

50. (New) A semiconductor capacitor comprising:

a bottom electrode formed over a substrate;

an insulating layer formed over said bottom electrode; and

a top electrode formed over said insulating layer, wherein at least one electrode surface comprises an electro-mechanically polished noble metal surface.

51. (New) A processor system comprising:

a processor; and

a memory device electrically coupled to said processor, said memory device comprising a substrate; and

a capacitor formed over said substrate, said capacitor comprising at least one electro-mechanically polished noble metal layer provided over said substrate.